Abstract of the Disclosure

Formation of elements of a vertical bipolar transistor is described, in particular a vertical npn transistor formed on a p-type substrate. Accordingly, an improved method not limited by constraints of photolithography, and an ensuing device made by such methods, is described. A temporary spacer (e.g., an oxide spacer) is deposited over a dielectric separation layer. The temporary spacer and dielectric separation layers are then anisotropically etched, forming a dielectric "boot shape" on a lower edge of the dielectric separation layer. An area within this non-photolithographically produced boot region defines an emitter contact window. Since the boot tip is formed through deposition and etching techniques, the emitter window is automatically aligned (i.e., self-aligned) with an underlying base region. Feature sizes are determined by deposition and etching techniques. Consequently, photolithography of small features is eliminated.